A new digital attenuator system for hybrid computers

by CONRAD PAUL PRACHT

CONRAD P. PRACHT was born in 1939 in Brocton, Illinois and spent his first years in the suburbs of Washington, D.C. After completing high school in Fairfax County, Virginia he entered the United States Army—to see the world. After a short basic training at Fort Knox, Kentucky he was sent to Fort Meade, Maryland, only 30 miles from home. C'est la vie.

He began college at Virginia Polytechnic Institute at Blacksburg, Virginia in 1959. As a co-op student he alternated between studies in Electrical Engineering at VPI and work in instrumentation at the U. S. Naval Weapons Laboratory at Dahlgren, Virginia. He received his BS degree from VPI in 1964, and joined the staff of NASA's Langley Research Center as an Aerospace Technologist.

Through his work in the Simulator Development Section of Langley's Analog Computer Branch, he developed an interest in analog/hybrid computation. After being accepted into NASA's graduate study program, he set out to continue his education (and see the country). Feeling that one could learn most about a subject from the author of books on the subject (and see more of the western U. S. by living there for a year or so), he chose to study under Dr. Granino Korn at the University of Arizona.

This paper is a direct result of his work as a research assistant in the U of A's Analog/Hybrid Computer Laboratory.

Mr. Pracht completed the requirements for the MS degree in Electrical Engineering in January, 1967 so he has now returned to his position at NASA-Langley.

He is a member of SCi, IEEE, Eta Kappa Nu, and Kappa Theta Epsilon. He is also an active and enthusiastic Kiwanian.

ABSTRACT

Digital attenuators are simple multiplying digital-to-analog converters used to replace coefficient-setting potentiometers in modern analog/hybrid computers. This report describes a new digital attenuator system employing low-phase-shift miniature metal-film ladder networks. They are switched by latching reed relays which give the system a nondestructive coefficient memory even when the computer is switched off. New digital control logic employs serial data transmission and requires only one address line per 14-bit attenuator. It permits one to set all 200 attenuators of a typical hybrid computer installation within 20 milliseconds. For maximum contact life, relay contacts are switched only when no current is flowing. The digital computer static-check routine can readily check individual relays to simplify maintenance.

Particular emphasis in this report is on a digital-attenuator system designed for a very fast repetitive computer in the Analog/Hybrid Computing Laboratory at the University of Arizona. The same design approach is readily applied to "slow" analog computers and appears to be even more advantageous there.

INTRODUCTION

In most electronic analog computers multiplication of voltages by constant coefficients has been implemented with potentiometers. In small computer systems, the potentiometers are set by hand. In larger systems employing 100 or more potentiometers, servo-setting systems are often used. Aside from being subject to mechanical wear and misadjustment, a servo potentiometer-setting system requires considerable time for setting. Potentiometers must be addressed and set one at a time. Usually, the desired coefficients are stored on punched paper tape, and the tape is read slowly until all potentiometers have been set. A typical setup time for 100 potentiometers is 12 minutes.[1] Digital attenuators are much faster, thereby greatly reducing problem setup time.

A typical digital attenuator system consists of a digital computer or tape-reading system for storing coefficient settings, an address network for addressing individual attenuators, a manual switching system for setting coefficients manually, a buffer register, and many (100 to 500) digital attenuator networks (figure 1).

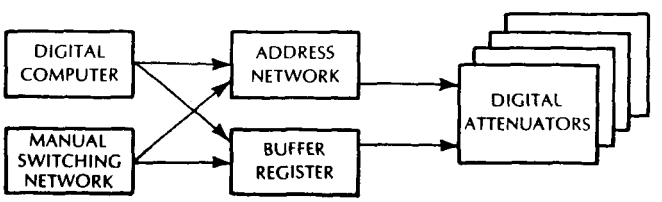


Figure 1 – A digital attenuator system

Each digital attenuator is, essentially, a multiplying digital-to-analog converter, which can be set to any desired coefficient. After the coefficient has been set, the analog input voltage is applied as the reference voltage on the digital-to-analog converter, which scales it down by the desired ratio (figure 2).

There are several obvious advantages to a digital attenuator system:

(1) Perhaps the most significant is that the system has no mechanical parts, with the possible exception of relays.

(2) Coefficients are set by digitally-controlled switches, instead of by a slow electromechanical servo system.

(3) Digital-attenuator setting intrinsically accounts for the effect of the load on the attenuator, while setting of a potentiometer requires feedback of the output voltage with the load connected. Hence, the digital attenuators can be set even before the computer patch panels have been put in place.

Several versions of the digital attenuator are already on the market, but, like anything new, they still suffer from various handicaps. Some require a separate amplifier for each attenuator. This is quite costly, as one amplifier or integrator may have as inputs the outputs of several digital attenuators. All present systems address all of the bits (usually 14) of each digital attenuator register in parallel. This results in complex and expensive address logic requiring multiple connections to every attenuator.

Another possible handicap, when relay switching is employed, is the large amount of current required by the coils of 1400 relays in 100 digital attenuators. Electronic switching is much faster, but the nonzero resistance of the switch presents difficulties, especially in fast low-impedance analog computers. One commercially available system employs electronic (FET) switches rather than relays. To reduce the error caused by the nonzero switch resistance, this system employs error feedback to adjust the least significant bits of the digital-to-analog converter network.

The new digital attenuator system described here attempts to overcome the above handicaps while keeping costs down to a practical figure.

TABLE OF SPECIFICATIONS

Specifications are given not only for the digital attenuator designed in this paper, which was built for a very fast repetitive computer, but also for a typical digital attenuator that might be built for a "slow" analog computer.

	Fast computer	Slow computer
Number of bits	14	16
Static accuracy	.02% of half scale	.02% of half scale
Resolution	.02% of half scale	.01% of half scale
Gain range	0.0002-3.2767	0.0001-13.1071
Feedback resistance	10K	1M
Ladder resistance	2.0514K	50K
Maximum load	13.3ma	4ma
Setting time per 200 attenuators	20 msec	20 msec

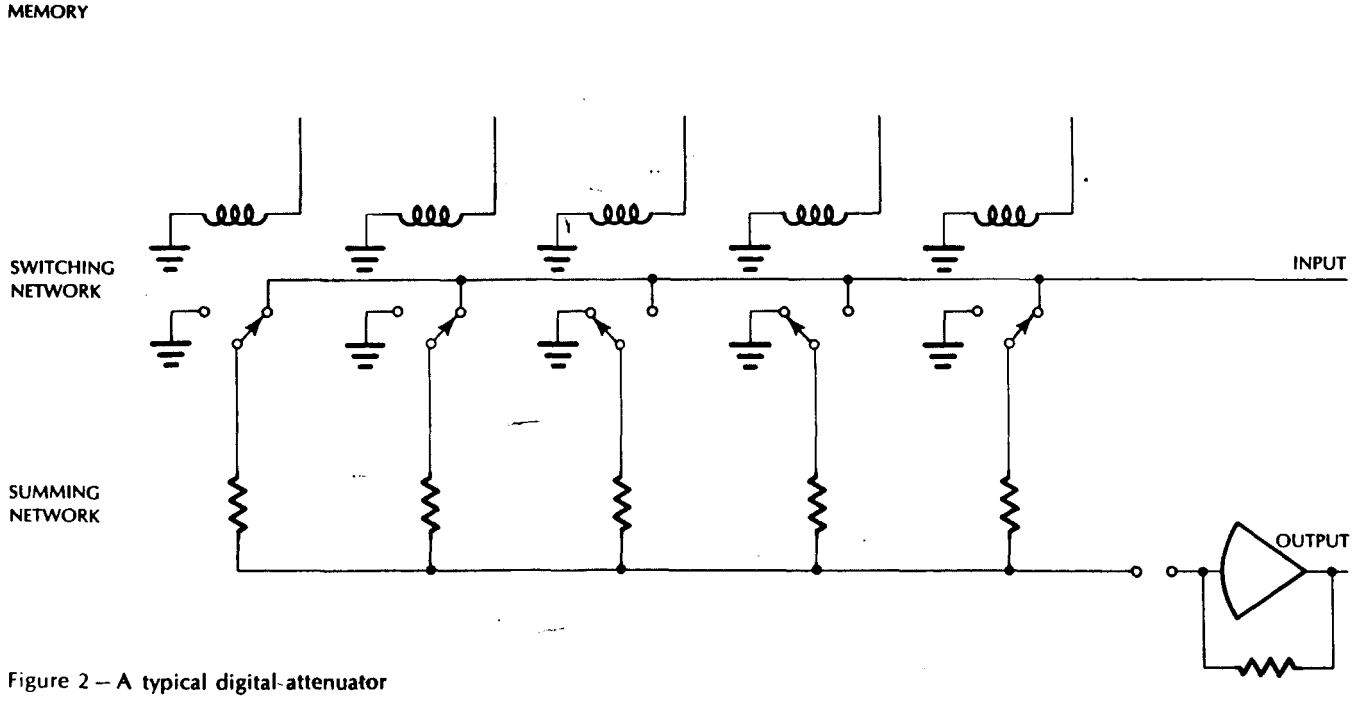


Figure 2 – A typical digital-attenuator

DESIGN OF A DIGITAL ATTENUATOR SYSTEM

To develop a digital attenuator is no simple task, for many of the requirements are conflicting, as the following list of design goals shows.

1. *Individual digital attenuators should not require separate amplifiers.* In other words, they should be capable of being patched into any amplifier or integrator.
2. Total setting time should not exceed 0.5 seconds.
3. *Transmission of data should be serial.* Parallel entry requires one address-gate tree for *each bit* of *each* digital attenuator; serial entry requires only a single address-gate tree for each digital attenuator. (This goal conflicts with goal number 2.)
4. *The load on the amplifier driving an attenuator network must not exceed that of a comparable coefficient-setting potentiometer.*
5. *The digital attenuator should have a range of coefficient settings from 0.0001 to at least 3.0.*
6. *A digital attenuator must not reduce the feedback ratio, β, of the succeeding amplifier more than a coefficient-setting potentiometer would.*
7. *The attenuator network should not require any adjustments.*

Having accepted the requirements that the digital attenuator be patchable and capable of accepting data serially, the design procedure was separated into four areas:

1. Attenuator network
2. Switches
3. Memory and addressing network
4. Control logic

These four areas will be discussed in detail.

The attenuator network

The function of the attenuator network is to convert an input voltage to a properly scaled summing-junction current, (figure 3). The first question to be considered is the choice between *binary weighting* and *binary-coded-decimal weighting.* Binary weighting was selected for reasons to be considered later; consequently, only binary networks will be discussed.

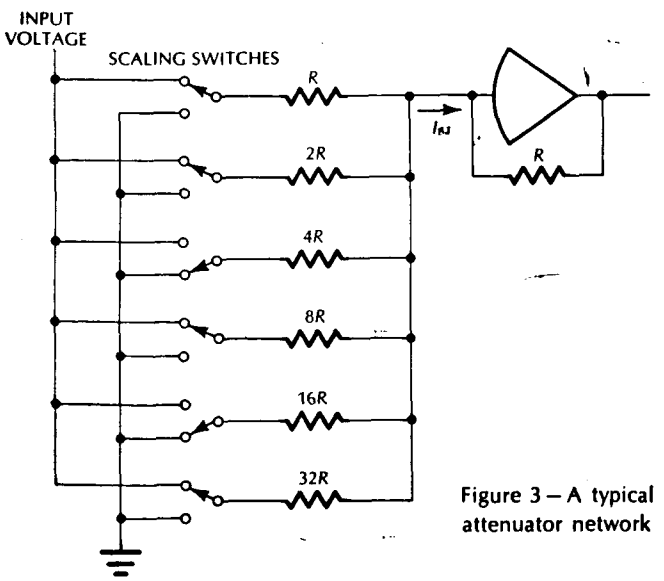
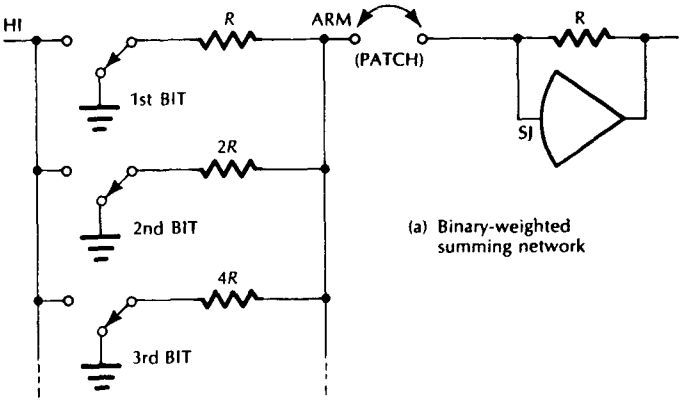
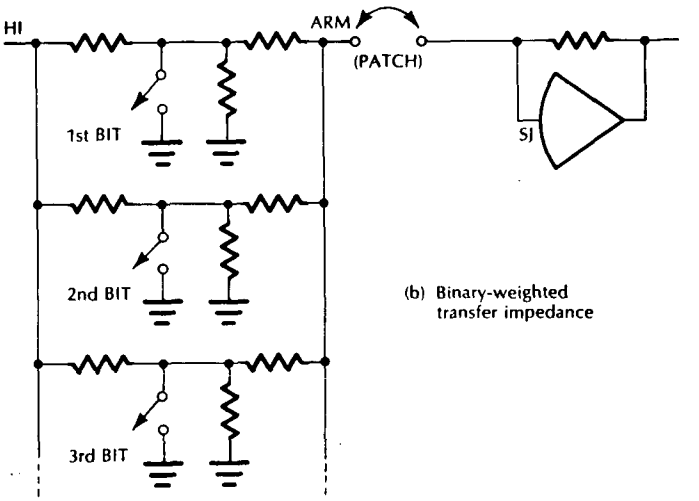


Figure 3 – A typical attenuator network

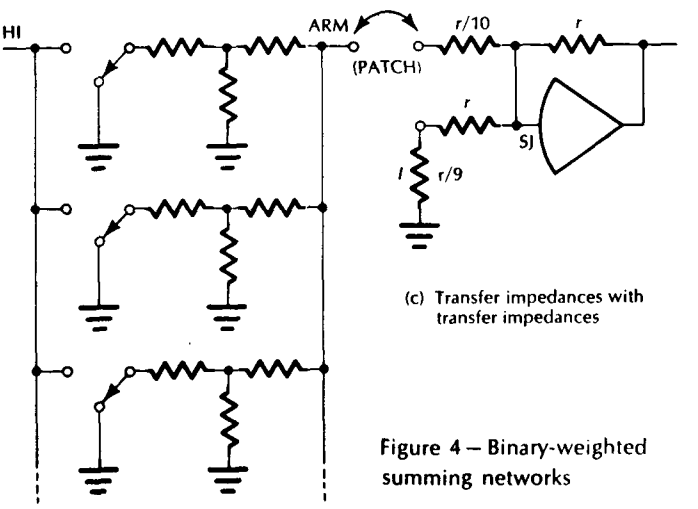
Figure 4 illustrates some binary-weighted attenuator designs;[2] many others are possible. Figure 4a shows a simple binary-weighted summing network employing SPDT (form C) relays to prevent capacitive feedthrough. Since the required 2^{14}:1 resistance ratio is not practical, the low-current branches may be implemented with T-network transfer impedances[3] (figure 4b). This network also permits use of the somewhat less expensive SPST (form A or B) relays. Both figures 4a and 4b employ *summing-junction patching,* which should work well for "slow" analog computers, but may not be practical for very fast repetitive computers.



(a) Binary-weighted summing network



(b) Binary-weighted transfer impedance



(c) Transfer impedances with transfer impedances

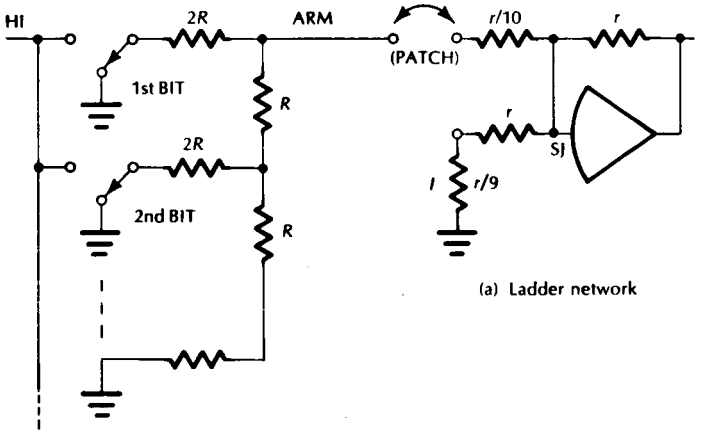
Figure 4 – Binary-weighted summing networks

The circuit of figure 4c permits patching to either gain-of-1 or gain-of-10 amplifier inputs if the latter are loaded as shown. The simple ladder network of figure 5 can be similarly patched and permits especially simple construction, since an entire *set* of similar metal-film resistors can be deposited on a ceramic substrate in a single operation.

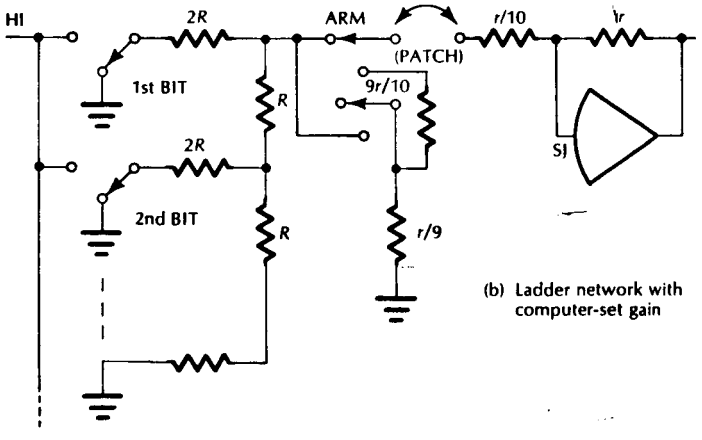
To simplify patching, the configuration in figure 5a can be rearranged as in figure 5b, and the digital computer can be employed not only to set the coefficient but also to set the gain (1 or 10). This network provides isolation from the summing junction, and the patching is always made to a gain-of-10 input.

The choice of resistance values in figures 4 and 5 must satisfy the following requirements:

1. The load on the driving amplifier must not be greater than that of a comparable coefficient potentiometer.
2. The summing-junction-to-ground impedance must not be so low that it excessively reduces the operational amplifier's feedback ratio and hence its bandwidth.
3. The impedances associated with the attenuator must not be so high that distributed capacitances unduly attenuate high frequencies; the phase shift of the digital attenuator should be less than that of a coefficient potentiometer.



(a) Ladder network



(b) Ladder network with computer-set gain

Figure 5 – Binary-weighted-ladder summing networks

The capacitances associated with high impedances (above 30K ohms) tend to lower the frequency response of very fast repetitive computers. For this reason, the feedback resistor for the amplifier was selected as 10K, and an upper limit of 30K was placed on attenuator resistors.

To demonstrate one of the tradeoffs in designing an attenuator network, consider a binary-weighted digital attenuator with only its most significant bit energized. In this case the output voltage represents one-half the maximum coefficient setting. The maximum coefficient of a binary-weighted ladder is always a power of two times its minimum coefficient (almost). For an attenuator to handle a coefficient setting of 10, in increments of 0.0001 it must be able to go to 13.1071 (a ratio of 1 to $2^{12}-1$).

With a given feedback resistor, $R_F = 10K$, and a given input, $E_{in} = 1$ volt, the transfer equation of the amplifier in figure 6 can be solved for the input and ladder resistances, R_I and R, thus establishing a relationship between them and the output. Numerically

$$R + R_I = -\frac{R_F}{2}\frac{E_{in}}{E_{out}} = -\frac{5000}{E_{out}}$$

Thus, if a maximum coefficient setting of 10 were mandatory, 13.1071 must be the design value of the largest coefficient, and the output with only the most significant bit energized would be — 6.5535 volts. This would require that $R + R_I = 762.9$ ohms.

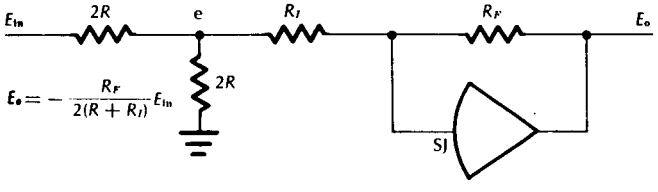


Figure 6 – Binary-weighted digital attenuator

To modify this design for a "slow" analog computer the following would apply:

1. If summing-junction patching is permitted, the input resistor, R_I, could be reduced to zero. This allows all of the resistance to be in the attenuator network, thereby reducing the load on the driving amplifier.
2. "Slow" computer design permits the feedback resistor to be as high as 100K. This, in turn, permits the ladder resistances to be much higher, thus greatly reducing the load on the driving amplifier and making higher coefficient settings possible.

Unfortunately, for a very fast computer a feedback resistor of at most 10K is mandatory, and summing-junction patching is prohibited; therefore, to achieve a coefficient-setting of 10 we must require that $R + R_I = 762.9$ ohms. The maximum load on an amplifier driving a 2000-ohm potentiometer set at 1.000 and connected to a 1000-ohm input resistor is 670 ohms. The minimum input impedance of a ladder network is approximately $R/2$.[4] To maintain the potentiometer loading conditions, the ladder resistance R must then be at least 1340 ohms. This conflict must be resolved.

The effect of the total resistance R_T (where $R_T = R + R_I$) on the maximum coefficient setting is shown in the following table:

Maximum Coefficient	$R_T = R + R_I$	Resolution
16.383	610.3	.1%
13.1072	762.9	.01%
8.191	1220	.1%
6.5536	1525.7	.01%
4.095	2440	.1%
3.2767	3051.4	.01%
2.047	4882	.1%
1.6383	6103	.01%

Since R_I, the input resistor, must be at least 1K (a gain-of-10 input), if R is to be at least 1.5K, the best configuration is the sixth entry, with a maximum coefficient setting of 3.2767, which meets the design goal of 3.0. R_I may be 1K with R then 2.0514K.

After considering all of the compromises, it was decided to design a digital attenuator containing 14 bits with a maximum coefficient of 3.2767 with .02% resolution. A ladder network with $R = 2051.4$ ohms and an input-output accuracy of .01% ± 5 ppm/°C was selected as the attenuator network.

A significant monetary savings can be realized by taking advantage of the fact that the accuracy of the less-significant-bit resistors of the ladder have very little effect on the transfer function. Thus a 14-bit ladder network can be constructed from two 7-bit ladder networks, one of the desired accuracy and one of a lower accuracy. This approach can be extended so that several ladders of decreasing accuracy are used.

When a coefficient greater than 3.2767 is required, a free amplifier must ordinarily be committed. It is possible, however, to parallel two attenuators, which adds their separate coefficient settings.

To improve network compromises, some existing digital attenuator systems associate an amplifier with each attenuator.[5] If the additional cost of such an amplifier is accepted, it would seem desirable to switch the feedback network rather than the input network, so that the amplifier offset and noise are not amplified along with the signal (figure 7).

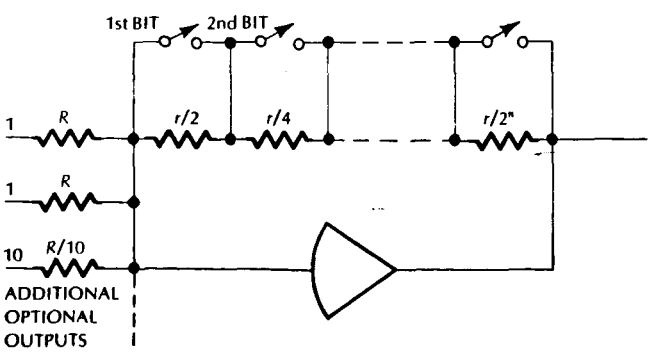


Figure 7 — Simple version of a summing amplifier with switched gain

The switches

Ladder networks (figures 5a and 5b) require SPDT switches, which are somewhat more expensive than SPST switches. These switches may be either electronic switches or relays.

FET electronic switches are very fast and are probably sufficiently accurate for slow analog computers, but the low impedances associated with a fast repetitive computer make the switch impedance significant. This non-negligible forward resistance may necessitate periodic adjustment of the resistors in the most significant bits of the ladder network. An alternative, as noted earlier, is to use error feedback to make adjustments necessitated by the switch impedances (figure 8).

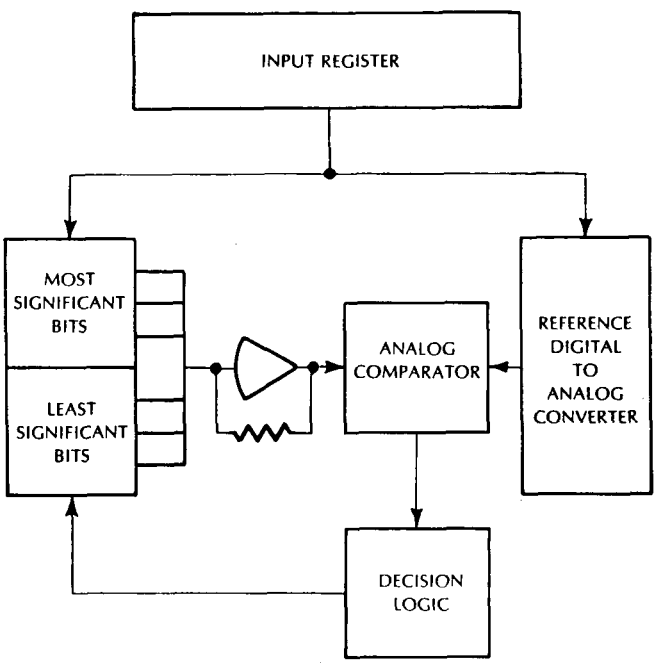


Figure 8 — Simplified block diagram of a digital attenuator employing error feedback

Reed relays have very low ON impedance and are generally less expensive than high-quality electronic switches, but they are much slower. One available relay has a settling time of from 3 to 5 milliseconds, while an electronic switch can be operated at microsecond speeds. Relays have the limited life of mechanical devices, but if they are operated "dry" (with the contacts not carrying current), their expected lifetime is acceptable (about 10^8 operations).[6]

Relays do offer an additional advantage: they are available in a form that employs magnetic latching, thereby making the relay not only a switch but also a memory device. Magnetic latching relays permit the relay-coil power to be turned off except when the analog computer is in the POT SET mode. This eliminates considerable power consumption, with the attendant heat dissipation, at only slight additional cost. The freedom to ground the relay-coil lines in the COMPUTE mode should also reduce digital noise in hybrid computers.

Memory and addressing system

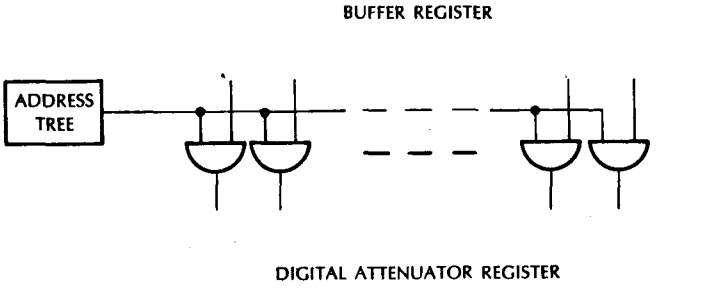
Since a digital attenuator must retain the desired coefficient after setting, it must have memory. This can be achieved several ways. A previously mentioned way is the use of magnetic latching relays and a single relay driver for all relays. While this technique is undoubtedly the least expensive, it is relatively slow, probably requiring 7 seconds or so to set 100 attenuators. What is worse, this technique requires separate addressing of each relay of each attenuator.

No doubt the fastest technique would be to use flip-flops for memory and electronic switches for analog switching. This would permit 100 attenuators to be set in a few milliseconds at most, but we would be forced to contend with the finite ON impedance of the electronic switches.

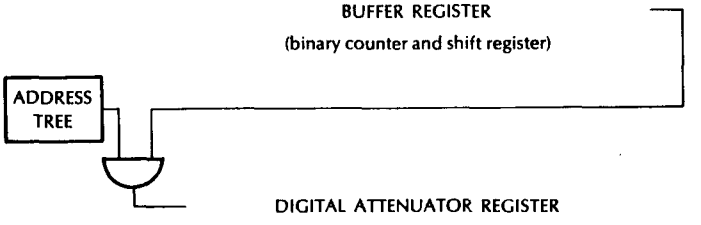
A compromise between the two aforementioned techniques eliminates many of their disadvantages. It is the use of a *flip-flop as the memory element together with a reed relay as the switch* (figure 9). *This technique enables the digital control system to set each flip-flop in about 10 microseconds and then continue on to the next attenuator, without having to wait for each relay to settle. Using this technique, all attenuators can be set in little more time than is required to set a single relay. This system is, in fact, so fast that it becomes possible to combine the relay-driving flip-flops for each attenuator into a shift register with serial input.* This greatly simplifies the digital attenuator's addressing scheme, requiring only one line per attenuator instead of 14 to 16, thus greatly reducing the cost (figure 10).

At a shift rate of 100K Hz and a relay settling time of 5 milliseconds, 100 attenuators can be set in only 20 milliseconds—while the computer operator is moving his hand from the POT SET switch to the COMPUTE switch.

A further refinement of the above technique once again uses magnetic latching relays, so that in the COMPUTE mode the power to the flip-flops driving the relays can be disconnected. This also permits the memory to be retained *even if the computer power is cut off,* reducing both digital noise and excess heat.



(a) Parallel addressing—14 lines and 14 gates to every attenuator



(b) Serial addressing—only one gate and one line to each attenuator

Figure 10 – A comparison of serial and parallel addressing

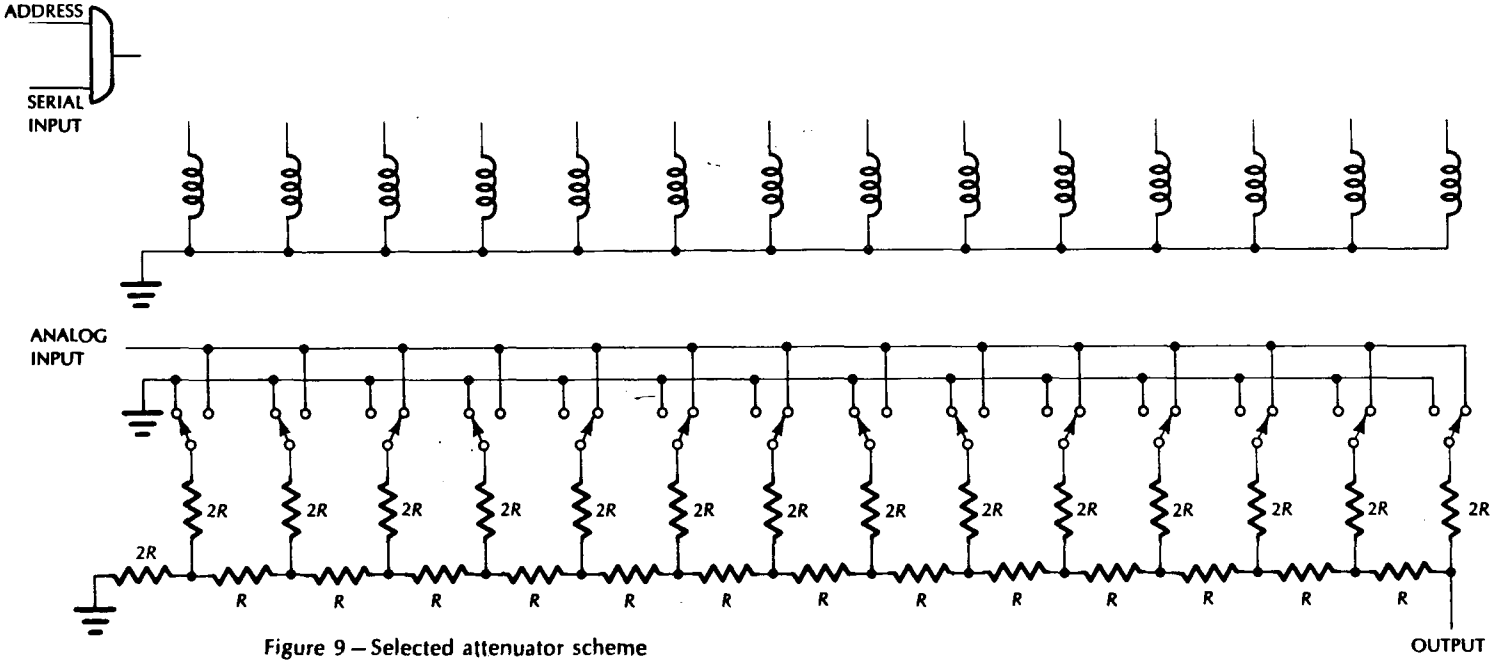


Figure 9 – Selected attenuator scheme

The control logic

Each digital attenuator must be capable of being set by both the digital computer and the manual coefficient-setting network on the computer control panel. Manual setting favors binary-coded decimal weighting of the digital attenuator network, while most digital computers favor binary weighting. Since the use of BCD weighting requires three additional bits per attenuator and thus three more relays per attenuator, binary weighting is much less expensive for any large number of attenuators. Therefore, binary weighting was chosen.

Binary weighting necessitates using a binary buffer register. When the digital computer sets the attenuator, it transfers stored addresses and coefficient settings in parallel to the buffer register. The addressing tree opens the logic to the correct attenuator, and the setting is shifted serially into the attenuator's register.

When setting attenuators manually, the decimal coefficient is set on BCD switches; it must first be converted to binary before it can be transferred to the buffer register. To do this, the manual BCD switches preset a BCD counter which counts the preset number of clock pulses, at a 100K Hz rate, into the same binary buffer register (which is also a counter) that accepts parallel entry from the digital computer (figure 11). Then the contents of the buffer register are shifted, as before, into the attenuator, which is now addressed by the manual address selector on the control console.

To set attenuators in the AUTOMATIC mode the operator must push a pushbutton switch to initiate the setting program. After all the attenuators have been set, the ATTENUATOR SETTING indicator light goes out. For MANUAL setting the operator must set the correct address and desired coefficient on the BCD switches and then push the pushbutton switch which initiates the manual setting routine.

The buffer register is used for both AUTOMATIC and MANUAL coefficient setting, but functions differently in each mode. In the AUTOMATIC mode, the register accepts parallel information from the digital computer output bus and then shifts the information serially to the correct attenuator. In the MANUAL mode, the register accepts and counts clock pulses until the preset BCD counter reaches zero; then it shifts its contents serially into the addressed attenuator. To implement these changes, a set of logic gates controls each individual flip-flop in the buffer register. These gates are controlled by the TRANSFER ENABLE, SHIFT ENABLE, and COUNT ENABLE signals shown in the simplified diagram of figure 12.

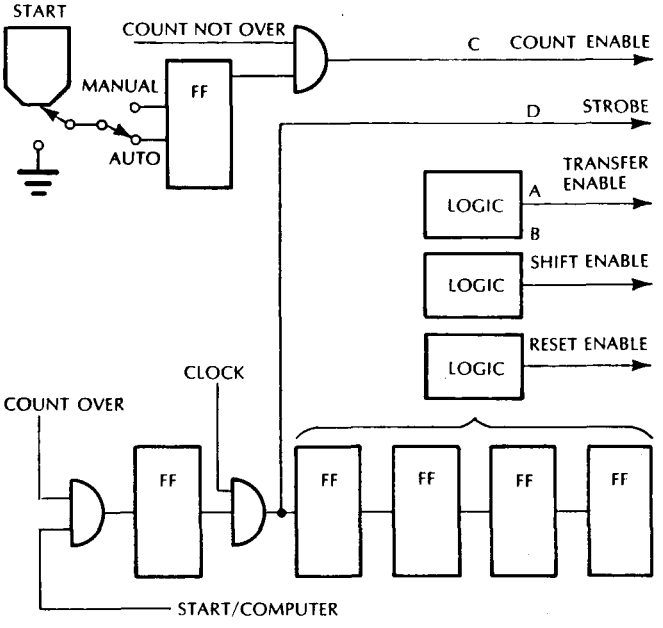


Figure 12 – Simplified timing logic

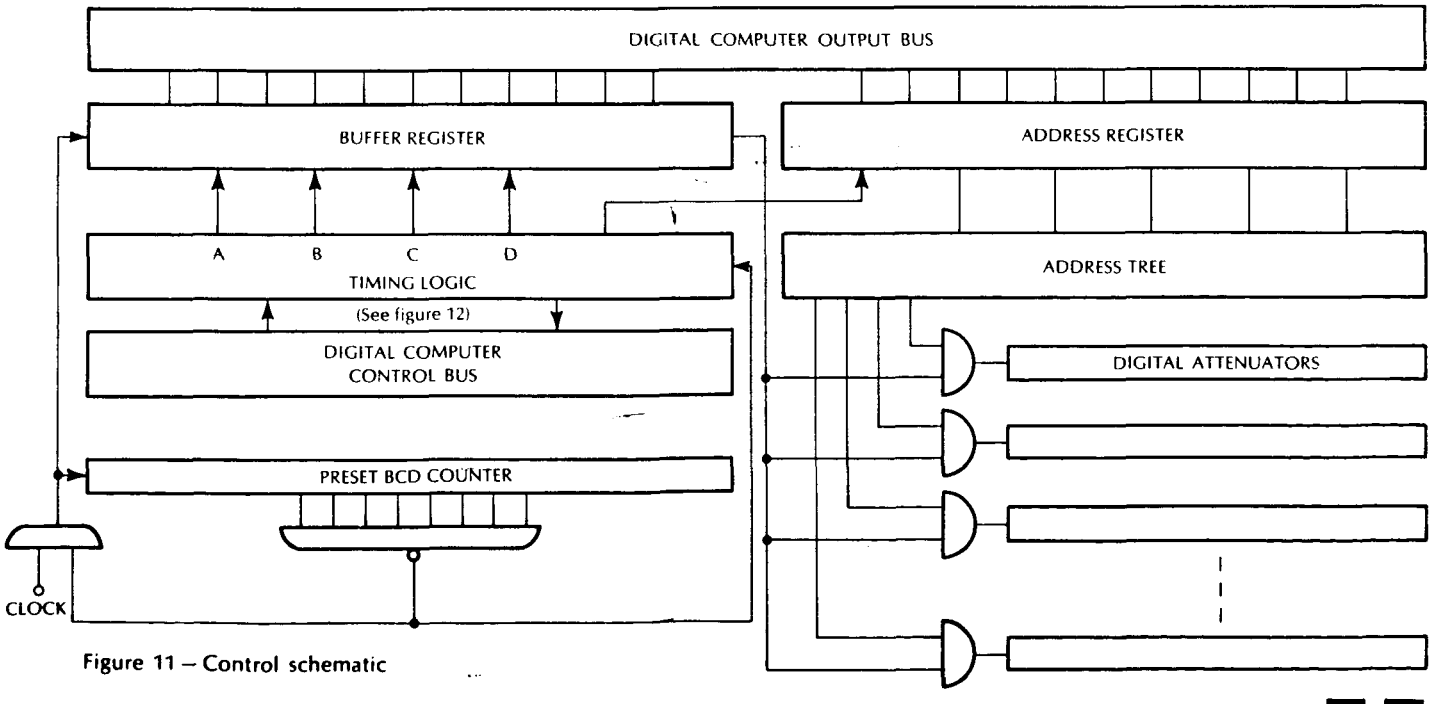


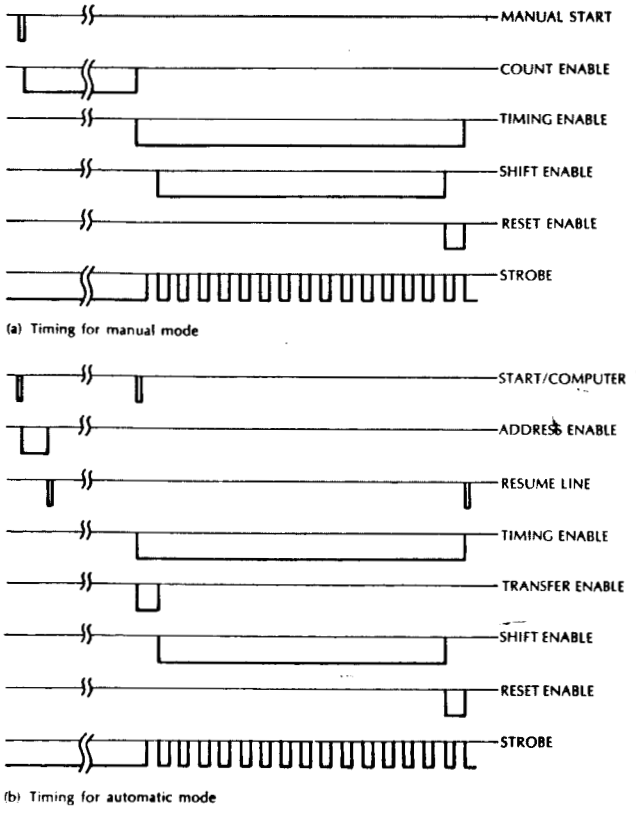
Figure 11 – Control schematic

The control signals for both the MANUAL and AUTOMATIC modes are compared in figure 13. Note that in either mode the last pulse resets all of the flip-flops in the control logic, and in the AUTOMATIC mode it also sends a signal back to the computer to show that the coefficient has been set. Appendix A contains a schematic diagram of a typical digital attenuator card.

Checking attenuator settings

Checking of attenuator settings is readily incorporated into the normal digital-computer-controlled static-check routine.[7] This routine is fairly slow, but it need only be run as part of normal static-check procedure. The digital computer can be programmed to print out setting errors and to test the attenuators involved to locate failed relays.

In the attenuator system which was built, each attenuator network is equipped with relays which connect the reference voltage (10 volts) to the input and connect the computer's digital voltmeter to the attenuator's output whenever the computer is in the MANUAL POT SET mode. The BCD switches for the address establish these connections, but as soon as the coefficient set pushbutton is energized, the reference voltage is removed; it is reconnected only after the attenuator has been set. In the MANUAL POT SET mode, each attenuator setting is read on the digital voltmeter as soon as the attenuator is addressed. The mode-control logic timing is shown in simplified form in figure 13.



(a) Timing for manual mode

(b) Timing for automatic mode

Figure 13 – Timing diagrams

Setting individual attenuators

It is often desirable to change the setting of only one attenuator, or of a few attenuators, in the course of a computation. With the very high setting speed of this new attenuator system, it would not take much more time to reset all attenuators each time a change is to be made; but this might invalidate past static checks and is also wasteful of digital-computer memory.

While it is easy to address any individual attenuator either manually or via the digital computer, individual-coefficient setting requires the capability for switching power to individual attenuator registers, so that the remaining coefficient settings remain undisturbed. This can take the form of one dry-switched relay or one gated emitter follower for each attenuator register. These devices are switched by the attenuator addressing tree, and can be mounted directly on the attenuator card.

Construction

This digital attenuator system has been built as described at the University of Arizona's Analog/Hybrid Computing Laboratory. The prototype digital attenuator card was custom made, and the control logic was implemented with Computer Controls Corporation general-purpose S-Pac logic elements.

A photograph of the attenuator card (figure 14) shows to what extent the physical size of the card depends on the reed relays. Magnetic latching relays are now available in TO-5 cans. An attenuator card made using these relays and integrated flip-flops would be so small that it could be plugged directly into the rear of a standard analog-computer patchbay, thus doing away with all analog signal wiring that is necessary between potentiometers and the patchbay.

TESTING AND RESULTS

Tests were conducted to determine the setting speed, static accuracy, and frequency response of the typical attenuator-amplifier combination shown in Appendix A. The results were as follows:

Setting time	20 msec
Static accuracy	0.02%
Phase-shift error at	
100 Hz	—
1 KHz	0.2%
10 KHz	0.5%
20 KHz	1%

Comparison with the phase-shift measurements for gain-of-1 and gain-of-10 amplifiers indicate that the phase-shift error is primarily due to the amplifier in a fast low-impedance computer; however, in a "slow" analog computer the stray capacitances in combination with the higher impedances will tend to cause more phase-shift error than the amplifier causes.

In the low-impedance computer, the phase-shift errors of the attenuator-amplifier combination was found to be almost exactly the same as that of the corresponding potentiometer-amplifier combination.

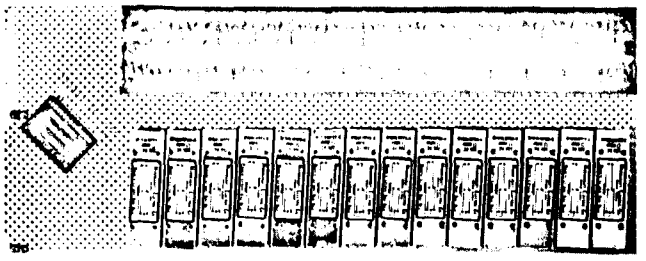


Figure 14 – Photograph of attenuator card

ACKNOWLEDGMENTS

The author wishes to acknowledge the encouragement, advice, and suggestions rendered by Professor Granino A. Korn in preparation of this thesis. He also is grateful to the National Aeronautics and Space Administration for their support under NASA Grant NsG-646 and under a NASA Institutional Grant to the University of Arizona, without which this project could not have been completed.

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APPENDIX A

Schematic of attenuator card